What is claimed is:

1. A checkerboard buffer page system, comprising:

a data source, providing data elements in a first order;

a data destination, receiving data elements in a second order;

at least two memory devices, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address, where data elements are stored in parallel to the memory devices and retrieved in parallel from the memory devices; and

where each data element corresponds to an entry in one of a plurality of buffer pages, each buffer page having a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order,

where data elements are stored to the memory devices in the first order and retrieved from the memory devices in the second order, and where at least one memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order,

where at least two data elements that are consecutive in the first order are stored in parallel to the memory devices, and

where at least two data elements that are consecutive in the second order are retrieved in parallel from the memory devices.

2. The checkerboard buffer page system of claim 1, further comprising a memory controller, where the memory controller generates addresses for storing and retrieving data elements, controls to which memory device to store which data element, and controls from which memory device to retrieve which data element.

3. The checkerboard buffer page system of claim 1, further comprising a first data switch and a second data switch, where the first data switch controls to which

memory device to store which data element, and the second data switch controls from which memory device to retrieve which data element.

4. The checkerboard buffer page system of claim 1, where each memory page in each memory device corresponds to a respective buffer page.

5. The checkerboard buffer page system of claim 1, where:

a data element is pixel data corresponding to a pixel in a frame of pixels, the frame having horizontal rows of pixels and vertical columns of pixels; and

the buffer pages are pixel pages, each pixel page having a plurality of pixel page rows and a plurality of pixel page columns.

6. The checkerboard buffer page system of claim 5, further comprising a memory controller, where the memory controller generates addresses for storing and retrieving data elements.

7. The checkerboard buffer page system of claim 6, where:

the at least two memory devices comprises a first memory device and a second memory device, and

the memory controller has two states for storing data for a horizontal pixel pair, where a first pixel in the horizontal pixel pair is horizontally adjacent and to the left of a second pixel in the horizontal pixel pair: a first state where pixel data for the first pixel in the horizontal pixel pair is stored to the first memory device and pixel data for the second pixel in the horizontal pixel pair is stored to the second memory device; and a second state where pixel data for the first pixel in the horizontal pixel pair is stored to the second memory device and pixel data for the second pixel in the horizontal pixel pair is stored to the first memory device.

8. The checkerboard buffer page system of claim 7, where the memory controller changes states for storing pixel data after storing data for one horizontal row of pixels.

9. The checkerboard buffer page system of claim 6, where:

the at least two memory devices comprises a first memory device and a second memory device, and

the memory controller has two states for retrieving data for a vertical pixel pair, where a first pixel in the vertical pixel pair is vertically adjacent and above a second pixel in the vertical pixel pair: a first state where pixel data for the first pixel in the vertical pixel pair is retrieved from the first memory device and pixel data for the second pixel in the vertical pixel pair is retrieved from the second memory device; and a second state where pixel data for the first pixel in the vertical pixel pair is retrieved from the second memory device and pixel data for the second pixel in the vertical pixel pair is retrieved from the first memory device.

10. The checkerboard buffer page system of claim 9, where:

pixel data for the first pixel in the vertical pixel pair is retrieved using a first address,

pixel data for the second pixel in the vertical pixel pair is retrieved using a second address,

in the first state for retrieving data, the first address is provided to the first memory device and the second address is provided to the second memory device, and

in the second state for retrieving data, the first address is provided to the second memory device and the second address is provided to the first memory device.

11. The checkerboard buffer page system of claim 9, where the memory controller changes states for retrieving data after retrieving pixel data for one vertical column of pixels.

12. The checkerboard buffer page system of claim 6, where:

the at least two memory devices comprises a first memory device and a second memory device, and

the memory controller has two states for storing data for a vertical pixel pair, where a first pixel in the vertical pixel pair is vertically adjacent and above a second pixel in the vertical pixel pair: a first state where pixel data for the first pixel in the vertical pixel pair is stored to the first memory device and pixel data for the second pixel in the vertical pixel pair is stored to the second memory device; and a second state where pixel data for the first pixel in the vertical pixel pair is stored to the second memory device and pixel data for the second pixel in the vertical pixel pair is stored to the first memory device.

13. The checkerboard buffer page system of claim 6, where:

the at least two memory devices comprises a first memory device and a second memory device, and

the memory controller has two states for retrieving data for a horizontal pixel pair, where a first pixel in the horizontal pixel pair is horizontally adjacent and to the left of a second pixel in the horizontal pixel pair: a first state where pixel data for the first pixel in the horizontal pixel pair is retrieved from the first memory device and pixel data for the second pixel in the horizontal pixel pair is retrieved from the second memory device; and a second state where pixel data for the first pixel in the horizontal pixel pair is retrieved from the second memory device and pixel data for the second pixel in the horizontal pixel pair is retrieved from the first memory device.

14. The checkerboard buffer page system of claim 5, further comprising a first data switch and a second data switch.

15. The checkerboard buffer page system of claim 14, where:

the at least two memory devices comprises a first memory device and a second memory device, and

the first data switch has two states for storing data for a pixel pair, where a first pixel in the pixel pair is horizontally adjacent and to the left of a second pixel in the pixel pair: a first state where pixel data for the first pixel in the pixel pair is stored to the first memory device and pixel data for the second pixel in the pixel pair is stored to the second memory device; and a second state where pixel data for the first pixel in a pixel pair is stored to the second memory device and pixel data for the second pixel in the pixel pair is stored to the first memory device.

16. The checkerboard buffer page system of claim 14, where:

the at least two memory devices comprises a first memory device and a second memory device, and

the second data switch has two states for retrieving data for a pixel pair, where a first pixel in the pixel pair is vertically adjacent and above a second pixel in the pixel pair: a first state where pixel data for the first pixel in the pixel pair is retrieved from the first memory device and pixel data for the second pixel in the pixel pair is retrieved from the second memory device; and a second state where pixel data for the first pixel in a pixel pair is retrieved from the second memory device and pixel data for the second pixel in the pixel pair is retrieved from the first memory device.

17. The checkerboard buffer page system of claim 16, where:

pixel data for the first pixel in the pixel pair is retrieved using a first address,

pixel data for the second pixel in the pixel pair is retrieved using a second address,

in the first state for retrieving data, the first address is provided to the first memory device and the second address is provided to the second memory device, and

in the second state for retrieving data, the first address is provided to the second memory device and the second address is provided to the first memory device.

18. The checkerboard buffer page system of claim 5, where at least two data elements that are consecutive in the first order are stored in parallel to sequentially the same memory page in each of the memory devices, and where at least two data elements

that are consecutive in the second order are retrieved in parallel from sequentially the same memory page in each of the memory devices.

19. The checkerboard buffer page system of claim 18, where the at least two data elements that are consecutive in the first order are stored using the same address.

20. The checkerboard buffer page system of claim 18, where the at least two data elements that are consecutive in the second order are retrieved using at least two addresses, and where each of the at least two addresses is different from another of the at least two addresses by the number of pixels in a pixel page row.

21. The checkerboard buffer page system of claim 5, where to which memory device to store pixel data for which pixel changes with each horizontal row of pixels.

22. The checkerboard buffer page system of claim 5, where from which memory device to retrieve which data element changes with each vertical column of pixels.

23. The checkerboard buffer page system of claim 5, where each row of the frame includes 1920 pixels and each column of the frame includes 1080 pixels.

24. The checkerboard buffer page system of claim 5, where a pixel page row includes 32 pixels and a pixel page column includes 16 pixels.

25. The checkerboard buffer page system of claim 5, where a pixel page includes pixels from multiple rows of the frame and pixels from multiple columns of the frame.

26. The checkerboard buffer page system of claim 25, where pixel data for at least two pixels adjacent in the first order is stored in the same memory page as pixel data for two pixels adjacent in the second order.

27. The checkerboard buffer page system of claim 5, where pixel data for pixels in one pixel page is stored in a single page of memory.

28. The checkerboard buffer page system of claim 5, further comprising at least one counter for generating addresses for storing and retrieving pixel data.

29. The checkerboard buffer page system of claim 28, where a counter counts pixels in the frame.

30. The checkerboard buffer page system of claim 28, further comprising a row counter and a column counter.

31. The checkerboard buffer page system of claim 28, further comprising a look-up-table of addresses, where a counter value is an index into the look-up-table of addresses.

32. The checkerboard buffer page system of claim 5, where pixel data is retrieved at twice or more than the rate pixel data is stored.

33. The checkerboard buffer page system of claim 32, where pixel data is stored at a rate supporting 60 frames per second, and pixel data is retrieved at a rate supporting 120 frames per second.

34. The checkerboard buffer page system of claim 32, where pixel data is retrieved for 64 pixels for every 32 pixels of pixel data that is stored.

35. The checkerboard buffer page system of claim 5 where the data destination is a grating light valve system including one or more grating light valves.

36. The checkerboard buffer page system of claim 35, where the frame is a high definition screen resolution frame having 1920 columns of pixels and 1080 rows of pixels per frame.

37. The checkerboard buffer page system of claim 35, where the grating light valve system includes three grating light valves, one for each of red, blue, and green.

38. The checkerboard buffer page system of claim 35, where each grating light valve sweeps one column at a time from left to right and from right to left in alternation.

39. The checkerboard buffer page system of claim 38, where a counter is used to generate addresses, and further where the counter increments as each grating light valve sweeps from left to right and the counter decrements as each grating light valve sweeps from right to left.

40. The checkerboard buffer page system of claim 5, where the data destination is a video processor.

41. The checkerboard buffer page system of claim 1, where at least one memory device is an 8MB 150 MHz SDRAM.

42. The checkerboard buffer page system of claim 1, where each memory device is divided into two memory sections, a first memory section for storing data elements and a second memory section for retrieving data elements.

43. The checkerboard buffer page system of claim 42, where a block of data elements is stored to the first memory sections of the memory devices and a block of data elements is retrieved from the second memory sections in alternation, and the memory sections switch roles between storing and retrieving.

44. The checkerboard buffer page system of claim 43, where a block of data elements is pixel data for a block of 32 pixels.

45. The checkerboard buffer page system of claim 42, where a counter is used for addressing, and where the counter is alternately reset to the beginning of the first sections or to the beginning of the second sections.

46. The checkerboard buffer page system of claim 1, where each memory device provides burst accessing.

47. A checkerboard pixel page system, comprising:

a video source providing pixel data for pixels in a frame, the frame having rows of pixels and columns of pixels;

a video destination;

a first memory having a plurality of memory locations;

a second memory having a plurality of memory locations;

a memory controller connected to the first memory and the second memory;

a first data bus connected to the video source and the memory controller;

a second data bus connected to the video source and the memory controller;

a third data bus connected to the video destination and the memory controller;

a fourth data bus connected to the video destination and the memory controller;

a source address line connected to the video source and the memory controller;

a destination address line connected to the video destination and the memory controller; and

where each pixel corresponds to an entry in one of a plurality of pixel pages, and a pixel page includes multiple pixels from a row in the frame and multiple pixels from a column in the frame,

where each entry in a pixel page corresponds to a memory location,

where pixel data for at least two pixels that are horizontally adjacent is stored in parallel to the memory devices, and

where pixel data for at least two pixels that are vertically adjacent is retrieved in parallel from the memory devices.

48. The checkerboard pixel page system of claim 47, where the memory controller generates addresses for storing and retrieving pixel data.

49. The checkerboard pixel page system of claim 47, where pixel data for a first half of the pixels in a pixel page is stored in the first memory and pixel data for a second half of the pixels in the pixel page is stored in the second memory.

50. The checkerboard pixel page system of claim 47, where pixel data for two pixels stored in parallel is stored at the same address in the first memory and the second memory.

51. A checkerboard buffer page system, comprising:

a data source, providing data elements in a first order;

a data destination, receiving data elements in a second order;

a buffer, including multiple memory pages, where the buffer stores multiple data elements in a memory page according to the first order and retrieves multiple data elements from the memory page according to the second order, and where the buffer stores multiple data elements in parallel to respective memory pages and retrieves multiple data elements in parallel from respective memory pages.

52. The checkerboard buffer page system of claim 51, where the data source is a video source.

53. The checkerboard buffer page system of claim 52, where the video source provides pixel data according to a high definition screen resolution having 1920 columns of pixels and 1080 rows of pixels per frame.

54. The checkerboard buffer page system of claim 51, where the data destination is a video display system.

55. The checkerboard buffer page system of claim 54, where the video display system is a grating light valve system including one or more grating light valves.

56. The checkerboard buffer page system of claim 51, where the data elements are pixel data for pixels in a frame, the first order is a horizontal row order, and the second order is a vertical column order.

57. The checkerboard buffer page system of claim 51, where the data elements are pixel data for pixels in a frame, the first order is a vertical column order, and the second order is a horizontal row order.

58. The checkerboard buffer page system of claim 51, where:

each data element corresponds to an entry in one of a plurality of buffer pages, each buffer page having a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order, and

each memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order.

59. A checkerboard pixel page system, comprising:

at least two memories for storing pixel data for pixels in a frame having rows and columns of pixels, where each memory includes multiple memory pages; and

a memory controller, where the memory controller stores and retrieves pixel data to the memories according to pixel pages, where each pixel page corresponds to a memory page in each of the memories and at least one pixel page includes pixels from multiple rows and pixels from multiple columns in the frame, and where the memory controller stores pixel

data for multiple pixels in parallel to respective memory pages and retrieves pixel data for multiple pixels in parallel from respective memory pages.

60. A method of storing pixel data, comprising:

storing pixel data for a first pixel and a second pixel in parallel in a first memory and a second memory, respectively, where the first pixel and the second pixel are pixels in a frame of pixels, where the frame includes multiple horizontal rows of pixels, and where the first pixel is the leftmost pixel in the first horizontal row of pixels in the frame and the second pixel is horizontally adjacent to the first pixel;

storing pixel data for a third pixel and a fourth pixel in parallel in the second memory and the first memory, respectively, where the third pixel is the leftmost pixel in the second horizontal row of pixels in the frame and is vertically adjacent to the first pixel, and the fourth pixel is horizontally adjacent to the third pixel; and

where pixel data for the first pixel and the fourth pixel is stored in the same memory page in the first memory, and

where pixel data for the second pixel and the third pixel is stored in the same memory page in the second memory.

61. The method of claim 60, further comprising:

providing pixel data from a video source to a memory controller;

generating a source address in the memory controller, where the source address is a memory address for storing the pixel data;

providing the pixel data to the first memory and the second memory;

providing the source address to the first memory and the second memory; and

storing the pixel data in the first memory and the second memory at the source address.

62. A method of retrieving pixel data, comprising:

retrieving pixel data for a first pixel and a second pixel in parallel from a first memory and a second memory, respectively, where the first pixel and the second pixel are

pixels in a frame of pixels, where the frame includes multiple horizontal rows of pixels and multiple vertical columns of pixels, and where the first pixel is the topmost pixel in the first vertical column of pixels in the frame and the second pixel is vertically adjacent to the first pixel;

retrieving pixel data for a third pixel and a fourth pixel in parallel from the second memory and the first memory, respectively, where the third pixel is the topmost pixel in the second vertical column of pixels in the frame and is horizontally adjacent to the first pixel, and the fourth pixel is vertically adjacent to the third pixel; and

where pixel data for the first pixel and the fourth pixel is stored in the same memory page in the first memory, and

where pixel data for the second pixel and the third pixel is stored in the same memory page in the second memory.

63. The method of claim 62, further comprising:

generating a first destination address and a second destination address in a memory controller, where each destination address is a memory address for retrieving pixel data;

providing the first destination address to the first memory;

providing the second destination address to the second memory;

providing pixel data from the first memory stored at the first destination address to the memory controller; and

providing pixel data from the second memory stored at the second destination address to the memory controller.

64. A method of storing data, comprising:

storing a first data element and a second data element in parallel in a first memory and a second memory, respectively, where the second data element is the next consecutive data element after the first data element in a first order of data elements;

storing data element data for a third data element and a fourth data element in parallel in the second memory and the first memory, respectively, where the fourth data element is the next consecutive data element after the third data element in the first order of

data elements, and where the third data element is the next consecutive data element after the first data element in a second order of data elements; and

where the first data element and the fourth data element are stored in the same memory page in the first memory, and

where the second data element and the third data element are stored in the same memory page in the second memory.

65. A system for storing pixel data, comprising:

means for storing pixel data for a first pixel and a second pixel in parallel in a first memory and a second memory, respectively, where the first pixel and the second pixel are pixels in a frame of pixels, where the frame includes multiple horizontal rows of pixels, and where the first pixel is the leftmost pixel in the first horizontal row of pixels in the frame and the second pixel is horizontally adjacent to the first pixel;

means for storing pixel data for a third pixel and a fourth pixel in parallel in the second memory and the first memory, respectively, where the third pixel is the leftmost pixel in the second horizontal row of pixels in the frame and is vertically adjacent to the first pixel, and the fourth pixel is horizontally adjacent to the third pixel; and

where pixel data for the first pixel and the fourth pixel is stored in the same memory page in the first memory, and

where pixel data for the second pixel and the third pixel is stored in the same memory page in the second memory.

66. A system for retrieving pixel data, comprising:

means for retrieving pixel data for a first pixel and a second pixel in parallel from a first memory and a second memory, respectively, where the first pixel and the second pixel are pixels in a frame of pixels, where the frame includes multiple horizontal rows of pixels and multiple vertical columns of pixels, and where the first pixel is the topmost pixel in the first vertical column of pixels in the frame and the second pixel is vertically adjacent to the first pixel;

means for retrieving pixel data for a third pixel and a fourth pixel in parallel from the second memory and the first memory, respectively, where the third pixel is the topmost pixel in the second vertical column of pixels in the frame and is horizontally adjacent to the first pixel, and the fourth pixel is vertically adjacent to the third pixel; and

where pixel data for the first pixel and the fourth pixel is stored in the same memory page in the first memory, and

where pixel data for the second pixel and the third pixel is stored in the same memory page in the second memory.

67. A system for storing data, comprising:

means for storing a first data element and a second data element in parallel in a first memory and a second memory, respectively, where the second data element is the next consecutive data element after the first data element in a first order of data elements;

means for storing data element data for a third data element and a fourth data element in parallel in the second memory and the first memory, respectively, where the fourth data element is the next consecutive data element after the third data element in the first order of data elements, and where the third data element is the next consecutive data element after the first data element in a second order of data elements; and

where the first data element and the fourth data element are stored in the same memory page in the first memory, and

where the second data element and the third data element are stored in the same memory page in the second memory.